Claims

1. A method for efficiently implementing the CORDIC complex phasor rotation comprising the steps of:

implementing a CORDIC algorithm using successive stages;

computing an incremental angle of rotation based on an examination of a plurality of highest-order active bits within a binary representation of a complete rotation angle; and

performing an incremental rotation based the incremental angle of rotation.

2. The method of claim 1 further comprising:

removing the highest order-bits from the complete rotation angle to create a remaining rotation angle and computing a next incremental angle based upon examination of another examination of highest order bits for the remaining rotation angle;

performing a another incremental rotation based on the next incremental step; and

repeating the removing and performing steps until the complete rotation angle is achieved.

3. The method of claim 1 wherein the step of computing further comprises two or more arithmetic comparisons of the complete rotation angle.

4. The method of claim 3 wherein the step of performing the incremental rotation further comprises a step of multiplying the tangents of the angles which were selected using only the highest order bits.

5. The method of claim 1 wherein the steps are performed within one or more digital logic devices.

6. The method of claim 5 wherein the digital logic devices further comprise a systolic processor array.

7. The method of claim 2 wherein the step of computing further comprises a comparison of n highest-order active bits within the binary representation of the complete rotation angle with a plurality of possible magnitudes for the incremental angle of rotation and selecting one of the magnitudes which can be either positive or negative.

8. A method for efficiently implementing the CORDIC complex phasor rotation comprising the steps of:

computing an incremental angle of rotation based on an examination of a plurality of highest-order active bits within a binary representation of a complete rotation angle;

performing an incremental rotation based the incremental angle of rotation;

discarding the highest order bits from the complete rotation angle to obtain a resulting rotation angle comprising the lowest order its of the complete rotation angle;

sign extending the resulting rotation angle.

9. The method for efficiently implementing the CORDIC complex phasor rotation of claim 8 wherein the step of computing further comprises comparing the highest order bits with a set to determine a relative value for the incremental angle.

10. The method for efficiently implementing the CORDIC complex phasor rotation of claim 8 wherein the step of computing further comprises computing a present-stage rotation angle that is a difference between the complete rotation angle and the incremental angle of rotation.

11. The method for efficiently implementing the CORDIC complex phasor rotation of claim 10 wherein the step of sign extending further comprises using a negative sign when the lowest-order bits equals the sign bit of present-stage rotation angle and a positive sign when they are different

12. A device for implementing CORDIC complex phasor rotations comprising:

a plurality of compare stages (24) that receive an input angle and provide a comparison between the input angle and a rotational angle, each compare stage (24)

outputting a difference between the input angle and the rotational angle and also providing an output for the rotational angle; and

a plurality of rotation stages (22) that receive the rotational angles from the compares (24) and implement a phasor rotation based on an examination of a plurality of highest order bits within a binary representation of the input angle.

13. The device of claim 12 wherein the compare stages (24) compute the rotational angle as a power of two.

14. The device of claim 13 wherein the rotation stages (22) contain a multiplier that multiplies tangents of angles which angles were selected using only the highest order bits of the angles.

15. The device of claim 12 wherein the device is contained within one or more digital logic devices.

16. The device of claim 12 wherein the device is implemented within a systolic processor array.

17. The device of claim 12 wherein the compare stages (24) provide a comparison of n highest-order active bits within the binary representation of the input angle with a plurality of possible magnitudes for the rotational angle and selects one of the magnitudes which can be either positive or negative.